WHAT IS CLAIMED IS:

1. An active matrix display, comprising:

a plurality of pixels arranged in an array;

a first transistor and a second transistor associated with each pixel, the first and second transistors positioned within the array for controlling current flow through each pixel;

a light emitting diode associated with each pixel; and

a storage capacitor associated with each pixel, wherein, during a time period for establishment of a threshold voltage on the storage capacitor for the first transistor, a voltage equal to the sum of the threshold voltage and a voltage for compensating for turnoff of the second transistor is established on the storage capacitor.

2. The display as recited in claim 1, further comprising:

a plurality of signal lines associated with each pixel for carrying signals for controlling the first and second transistors; and

a plurality of power connections associated with each pixel for supplying power to each pixel.

3. The display as recited in claim 2, wherein a voltage on a positive connection of the plurality of power connections is greater than or equal to the total of a maximum voltage on a data signal line of the plurality of signal lines, a

maximum voltage on the light emitting diode, and a voltage on a negative connection of the plurality of power connections.

4. The display as recited in claim 3, wherein the maximum voltage on the data signal line corresponds to a maximum luminance of the light emitting diode.

5. The display as recited in claim 3, wherein a minimum voltage on the data signal line corresponds to zero luminance of the light emitting diode.

6. The display as recited in claim 3, wherein the voltage on the negative connection is greater than or equal to the total of the negative of a mimimun threshold voltage of the first transistor and the negative of an illumination onset voltage of the light emitting diode.

7. The display as recited in claim 3, wherein a voltage on a reverse bias connection of the plurality of power connections is less than the negative of a maximum threshold voltage of the first transistor.

8. The display as recited in claim 1, wherein the time period is between approximatley 100 microseconds and 200 microseconds.

9. The display as recited in claim 1, wherein the second transistor is turned on at a beginning of the time period and turned off at a predetermined point after the beginning and before an end of the time period.

10. The display as recited in claim 9, wherein the first transistor is turned on at the same time that the second transistor is turned off.

11. The display as recited in claim 9, further comprising a third transistor associated with each pixel that is turned on and off at the same time that the second transistor is turned on and off, respectively.

12. The display as recited in claim 1, wherein a voltage on the storage capacitor is reduced to establish the voltage equal to the sum of the threshold voltage for the first transistor and the voltage for compensating for turnoff of the second transistor.

13. The display as recited in claim 1, wherein the light emitting diode includes organic material.

14. The display as recited in claim 1, wherein the first and second transistors include thin-film transistors.

15. The display as recited in claim 14, wherein the thin-film transistors are made from amorphous silicon.

16. The display as recited in claim 2, wherein the plurality of signal lines includes a data signal line, a gate signal line, an on/off signal line, and a reverse bias voltage signal line.

17. The display as recited in claim 2, wherein:

the plurality of power connections includes a positive connection, a negative connection and reverse bias connection; and

the positive, negative and reverse bias connections do not change their respective voltage levels during the time period for establishment of the threshold voltage on the storage capacitor.

18. A method for obtaining threshold voltage compensation for an active matrix display, comprising:

providing a plurality of pixels arranged in an array, wherein each pixel includes a first transistor, a second transistor, a light emitting diode, and a storage capacitor associated therewith;

positioning the first and second transistors within the array for controlling current flow through each pixel; and

establishing on the storage capacitor a voltage equal to the sum of a threshold voltage for the first transistor and a voltage for compensating for turnoff of the second transistor.

19. The method as recited in claim 18, wherein the step of establishing occurs during a time period for establishment of the threshold voltage for the first transistor.

20. The method as recited in claim 18, wherein each pixel includes a plurality of signal lines associated therewith for carrying signals for controlling the first and second transistors, and each pixel includes a plurality of power connections associated therewith for supplying power to each pixel.

21. The method as recited in claim 20, wherein a voltage on a positive connection of the plurality of power connections is greater than or equal to the total of a maximum voltage on a data signal line of the plurality of signal lines, a maximum voltage on the light emitting diode, and a voltage on a negative connection of the plurality of power connections.

22. The method as recited in claim 21, wherein the maximum voltage on the data signal line corresponds to a maximum luminance of the light emitting diode.

23. The method as recited in claim 21, wherein a minimum voltage on the data signal line corresponds to zero luminance of the light emitting diode.

24. The method as recited in claim 21, wherein the voltage on the negative connection is greater than or equal to the total of the negative of a mimimun threshold voltage of the first transistor and the negative of an illumination onset voltage of the light emitting diode.

25. The method as recited in claim 21, wherein a voltage on a reverse bias connection of the plurality of power connections is less than the negative of a maximum threshold voltage of the first transistor.

26. The method as recited in claim 19, wherein the time period is between approximatley 100 microseconds and 200 microseconds.

27. The method as recited in claim 19, further comprising:

turning on the second transistor at a beginning of the time period; and

turning off the second transistor at a predetermined point after the beginning and before an end of the time period.

28. The method as recited in claim 27, further comprising turning on the first transistor at the same time that the second transistor is turned off.

29. The method as recited in claim 27, further comprising turning a third transistor associated with each pixel on and off at the same time that the second transistor is turned on and off, respectively.

30. The method as recited in claim 18, wherein the light emitting diode includes organic material.

31. The method as recited in claim 18, wherein the first and second transistors include thin-film transistors.

32. The method as recited in claim 31, wherein the thin-film transistors are made from amorphous silicon.

33. The method as recited in claim 20, wherein the plurality of signal lines includes a data signal line, a gate signal line, an on/off signal line, and a reverse bias voltage signal line.

34. The method as recited in claim 20, wherein the plurality of power connections includes a positive connection, a negative connection and reverse bias connection, and the method further comprises maintaining the respective voltage levels of the positive, negative and reverse bias connections during the time period for establishment of the threshold voltage on the storage capacitor.

35. An active matrix display, comprising:

a plurality of pixels arranged in an array;

at least three transistors associated with each pixel, the at least three transistors positioned within the array for controlling current flow through each pixel;

a light emitting diode associated with each pixel; and

a storage capacitor associated with each pixel, wherein, during a time period for establishment of a threshold voltage on the storage capacitor for a first transistor of the at least three transistors, a voltage of the storage capacitor is set to a voltage including the threshold voltage and a voltage for compensating for turnoff of a second transistor of the at least three transistors.

36. A method for obtaining threshold voltage compensation for an active matrix display, comprising:

providing a plurality of pixels arranged in an array, wherein each pixel includes at least three transistors, a light emitting diode, and a storage capacitor associated therewith;

positioning the at least three transistors within the array for controlling current flow through each pixel; and

establishing, during a time period for establishment of a threshold voltage of a first transistor of the at least three transistors on the storage capacitor, a voltage for compensating for turnoff of a second transistor of the at least three transistors on the storage capacitor.

37. A pixel circuit for an active matrix display, comprising:

at least three transistors for controlling current flow through a pixel;

a light emitting diode;

a plurality of signal lines for carrying signals for controlling the at least three transistors;

a plurality of power connections for supplying power to the pixel; and

a storage capacitor, wherein, during a time period for establishment of a threshold voltage on the storage capacitor for a first transistor of the at least three transistors, a voltage equal to the sum of the threshold voltage and a voltage for compensating for turnoff of a second transistor of the at least three transistors is established on the storage capacitor.